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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,406	03/31/2004	Vikram Magoon	ITL.1128US (P19039)	5392

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,406	MAGOON ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-26 are presented in the instant application according to the Applicants' filing on 03/31/2004.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Abstract

2. The abstract of the disclosure is objected to because of the length. Correction is required. See MPEP § 608.01(b).

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "**means**" and "**said**," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Oh et al. (U.S. Patent No. 6,882,233).

With respect to claim 1, Oh et al. discloses, in Fig. 5, a circuit and its corresponding method comprising selectively coupling capacitors of oscillator stages [(C51, C53, C55; M51, M53, M55); (C52, C54, C56; M52, M54, M56)] together to set an oscillation frequency.

With respect to claim 2, Oh et al. discloses, in Fig. 5, that the coupling comprises differentially coupling the capacitors together.

With respect to claim 3, Oh et al. discloses, in Fig. 5, each stage comprises multiple capacitors [(C51, C53, C55); (C52, C54, C56)], the method further comprising selectively coupling the capacitors together in pairs [C51,C52; C53,C54; C55,C56] to adjust the frequency.

With respect to claim 4, Oh et al. discloses, in Fig. 5, that the method further comprising binarily-weighting the capacitors.

With respect to claim 5, Oh et al. discloses, in Fig. 5, that the coupling comprises coupling one terminal of a capacitor from each stage together and coupling another terminal of the capacitor from each stage to an output terminal.

With respect to claim 6, Oh et al. discloses, in Fig. 5, that the method further comprising selectively coupling the capacitors to ground.

With respect to claim 7, Oh et al. discloses, in Fig. 5, that the step of selectively coupling the capacitors to ground comprises coupling the capacitors to ground when not being used to adjust the oscillation frequency.

With respect to claim 8, Oh et al. discloses, in Fig. 5, that the method further comprising using one of the oscillator stages [(C51, C53, C55; M51, M53, M55); (C52, C54, C56; M52, M54, M56)] to generate a first output signal; and using another one of the oscillator stages [(C51, C53, C55; M51, M53, M55); (C52, C54, C56; M52, M54, M56)] to generate a second signal orthogonal to the first signal.

With respect to claim 9, Oh et al. discloses, in Fig. 5, that the first and second oscillating signals have the same oscillation frequency.

6. Claims 10-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Sawada (U.S. Pub. No. 2003/0227341).

With respect to claim 10, Sawada discloses, in Fig. 5, a system comprising a first oscillator stage [Cf0, Cf1, Cv20, Cv21]; a second oscillator stage [Cf0, Cf1, Cv20, Cv21] and switches [S20, S21] to selectively couple capacitors of the first and second oscillator stages together to adjust an oscillation frequency.

With respect to claim 11, Sawada discloses, in Fig. 5, that the switches differentially couple the capacitors together.

With respect to claim 12, Sawada discloses, in Fig. 5, that each stage comprises multiple capacitors, wherein the switches selectively couple the capacitors together so that the capacitors when coupled together are connected in a pair.

With respect to claim 13, Sawada discloses, in Fig. 5, that the multiple capacitors are binarily-weighted.

With respect to claim 14, Sawada discloses, in Fig. 5, that the switches couple one terminal of a capacitor from each stage together and couple another terminal of the capacitor from each stage to an output terminal.

With respect to claim 15, Sawada further discloses, in Fig. 5, that additional switches [S30, S31] to selectively couple the capacitors to ground.

With respect to claim 16, Sawada further discloses, in Fig. 5, that the switches selectively couple the capacitors to ground that are not being used to adjust the oscillation frequency.

With respect to claim 17, Sawada further discloses, in Fig. 5, that the first oscillator stage generates a first output signal [OUTA], and the second oscillator stage generates a second signal [OUTB] orthogonal to the first signal.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (U.S. Patent No. 6,882,233) in view of Steubing et al. (U.S. Patent No. 5,233,232).

With respect to claims 18 and 21, Oh et al. discloses, in Fig. 5, a circuit and its corresponding method comprising a step of selectively activating capacitors [C51-C56] to adjust an oscillating frequency of an oscillator.

Oh et al. fails to specifically disclose that for each of the capacitors using parasitic capacitance as the main component of capacitance for the capacitor.

Steubing et al. discloses, in Fig. 6, col. 11, line 1 and col. 12, lines 1-2, capacitors [Q90, Q91] using parasitic capacitance as the main component of capacitance for the capacitor.

To configure the circuit of Oh et al. with capacitors using parasitic capacitance as the main component of capacitance for the capacitor as taught by Steubing et al. would have been obvious to one of ordinary skill in the art at the time of the invention since Steubing et al. teaches that such configuration would provide peaking at the outputs *(see Steubing et al. col. 12, lines 1-2).*

9. Claims 19-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (U.S. Patent No. 6,882,233) in view of Steubing et al. (U.S. Patent No. 5,233,232), as applied to claim 18, and further in view of Nakayama (JP. Patent No. 08148651A).

With respect to claims 19-20 and 22-23, the combined teaching of Oh et al. and Steubing discloses all of the claimed limitations as expressly recited in claims 18 and 21, except for the step of forming the capacitors from parasitic capacitance exhibited between metal layers of a semiconductor device and from metal-to-metal capacitors.

Nakayama discloses capacitors being formed based on parasitic capacitance from conductive layers in a semiconductor device *(see Title)*.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure a circuit based on the combined teaching of Oh et al. and Steubing et al. with capacitors formed from parasitic capacitance from metal layers as taught by Nakayama to facilitate the selected etching layering since such circuit arrangement of the circuit for the stated purpose has been a well known practice as evidenced by the teachings of Nakayama.

10. Claims 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Sawada (U.S. Pub. No. 2003/0227341) in view of Ravi et al. (U.S. Pub. No. 2004/0119547).

With respect to claims 24 and 25, Sawada discloses, in Fig. 5, a system comprising a first oscillator stage [Cf0, Cf1, Cv20, Cv21]; a second oscillator stage [Cf0, Cf1, Cv20, Cv21] and switches [S20, S21] to selectively couple capacitors of the first and second oscillator stages together to adjust an oscillation frequency.

Sawada fails to teach a wireless interface comprising a dipole antenna to communicate with a communication link in response to at least one oscillation signal provided by at least one of the first and second oscillator stages.

Ravi et al. discloses, in Fig. 1B, a wireless interface comprising a dipole antenna [60] to communicate with a communication link in response to a controlled oscillator stage [40].

To configure the circuit of Sawada with a wireless interface comprising a dipole antenna to communicate with a communication link in response to a controlled oscillator stage as taught by Anderson, Jr. et al. to provide multiple frequency bands usage would have been obvious to

one of ordinary skill in the art at the time of the invention since Ravi et al. teaches that such configuration would extend a tunable range of desirable frequency *(see Ravi et al., page 2, left col., first paragraph)*.

11. Claim 26 is rejected under 35 U.S.C. 102(e) as being anticipated by Sawada (U.S. Pub. No. 2003/0227341) in view of Ravi et al. (U.S. Pub. No. 2004/0119547), as applied in claim 24, and further in view of Sternberg (U.S. Patent No. 6,606,487).

With respect to claim 26, the combined teaching of Sawada and Ravi et al. discloses all the limitations as claimed in claim 24 except for a Discrete Fourier Transform engine.

Sternberg discloses applying Discrete Fourier Transform to estimate frequency error and update the oscillator circuit [Col. 1, lines 29-32].

To configure the circuit based on the combined teaching of Sawada and Ravi et al. of with the application of Discrete Fourier Transform to estimate frequency error and update the oscillator circuit as taught by Sternberg would have been obvious to one of ordinary skill in the art at the time of the invention since Sternberg teaches that such configuration would prevent significant out-of-band interference [col. 1, line 26-28].

Citation of Relevant Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Sano (U.S. Patent No. 6,828,868) discloses a semiconductor device having an oscillating circuit.

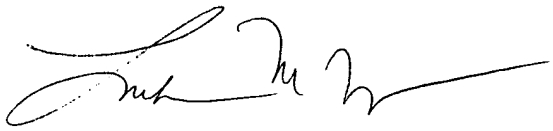
Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



LINH MY NGUYEN
PRIMARY EXAMINER